by Sedra and smith".

Applicants submit that independent claims 1, 12, and 23 are neither anticipated nor rendered obvious by Lee. It should be noted that, although not separately addressed herein, the dependent claims incorporate limitations that present patentable subject matter in their own right. However, in an attempt to present a more concise response to the OFFICE ACTION, only certain limitations or elements of independent claims 1, 12 and 23 are discussed below. No inference or conclusion of any kind should be drawn from the absence of comments pertaining to other limitations or elements, whether those limitations or elements are contained in independent or dependent claims.

Claim 1 is not Anticipated by Lee

In the OFFICE ACTION, claim 1 was rejected as being anticipated by Lee. Applicants respectfully submit that independent claim 1 is not anticipated by Lee. Claim 1 is directed towards an integrated circuit device and recites, in part:

> a bond pad structure including:
>
> a conductive pad;
>
> a first doped region... underlying and surrounding the conductive pad;
>
> a conductive region of the first conductivity type disposed in the first doped region...
>
> an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and
>
> a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.

Regarding claim 1, the OFFICE ACTION cites that "Lee discloses, figure 14, an integrated circuit device comprising: a conductive pad (I/O pad)... a first doped region 61 ... underlying and surrounding the conductive pad"[1] and that "Lee discloses in figure 14 that the I/O pad is connected to doped region 63. Therefore, 63 is essentially part of the I/O pad."[2]

Applicants respectfully disagree. The ESD transistor structure of Lee, Fig. 14, cited in the OFFICE ACTION as reading on the elements of claim 1, is not disclosed in Lee as comprising any portion of a bond pad structure. Generally speaking, transistor structures, such as the one included in the electrostatic discharge ("ESD") protection circuit disclosed in Fig. 14 of Lee are separate and mutually exclusive from bond pad structures found on contemporary semiconductor devices (i.e., to the extent known, they are not integrated together as part of the same vertical structure).

Claim 1 recites, among other things, that the doped region is underlying and surrounding the conductive pad. While applicants may agree that Lee discloses schematically that an "I/O pad" (Fig. 14) is connected to the source region 63, there simply is no disclosure in Lee that the source region 63 is "underlying and surrounding" any conductive pad layer (at least because Lee does not disclose the whereabouts of any such pad). Applicants simply do not see how the Lee reference can possibly indicate that "63 is essentially part of the I/O pad" as is cited in the OFFICE action because there is simply no such disclosure in Lee.

In addition, Applicants respectfully submit that the transistor of Lee, Fig. 14 (i.e., the transistor comprising segments "52, 53, and 54") which in the OFFICE ACTION is read as "an output driver transistor as recited in claim 1" is in fact not an "output driver" but rather a transistor used for ESD protection. (e.g., col. 4, lines 39-40 of Lee, "FIGS 10 to 21 are sectional

[1] OFFICE ACTION, page 2, item 2
[2] page 8 of the OFFICE ACTION, item 7, (section titled "Response to Arguments)

views showing the ESD protective circuit according to the present invention.")

Thus, for at least these reasons, Lee does not anticipate claim 1.

Claim 12 is not Obviated by Lee

In the OFFICE ACTION, claim 12 was rejected as being obvious in view of Lee. Claim 12 is directed to a bond pad for an integrated circuit device and recites in part:

> a conductive bonding layer;
>
> a doped region of a first conductivity type... underlying and surrounding the conductive bonding layer;
>
> a conductive region... underlying the conductive bonding layer and wherein the conductive region includes a surface area at least substantially equal to a surface area of the conductive bonding layer...

Regarding claim 12, the OFFICE ACTION cites that "Lee discloses the bond pad comprising bonding pad layers 63-65, a first doped region 61... underlying and surrounding the conductive bonding layer...". For at least the same reasons described above with respect to claim 1, Applicants submit that Lee does not disclose any such bond pad comprising any of the elements of claim 12. Rather Lee, in Fig. 14, simply illustrates sectional views of transistor structures for ESD which do not form any part of a bond pad. Lee, in Fig. 14, indicates that the ESD transistor structures are connected to an "I/O" pad by way of a symbol. No elements of any bond pad corresponding to this symbol are disclosed in Lee.

Thus, for at least this reason, Applicants submit that claim 12 is not anticipated or rendered obvious by Lee.

Claim 23 is not Obviated by Lee in view of Sakai

In the OFFICE ACTION, claim 23 was rejected as being obviated by Lee in view of Sakai. Applicants respectfully submit that independent claim 23 is not rendered obvious by Lee in view of Sakai. Claim 23 is directed to a transistor layout for an integrated circuit device having a bond pad and recites in part:

> a drain region having a first conductivity type doping...formed in a semiconductor substrate region having a second conductivity type doping, the drain region being electrically coupled to the bond pad;
>
> a source region including a second conductivity type doping; and
>
> a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically coupled to the source region, wherein a section of the conductive tap region is structurally integrated with the source region.

Regarding claim 23, the OFFICE action cites that, "Lee neither discloses the source and the drain region being of opposite conductivity types, nor discloses a section of the conductive tab region is [sic] structurally integrated with the source region" and that "it would be obvious to one of ordinary skill in the art to make the source and the drain region of the opposite conductivity type at the time of the invention to make the source and drain region of the opposite conductivity type, as the Japanese patent teaches, in order to be able to use Lee's invention in a memory device"[3].

Sakai, to the extent understood, is directed to a Read-Only Memory ("ROM") whose memory cell transistors include "isolation regions" to isolate source and drain regions from gate regions. Lee is directed to electrostatic discharge protection ("ESD") circuitry related to protecting a semiconductor device from electrostatic discharge "injected through an input

[3] OFFICE ACTION, page 6, item 5

terminal of the semiconductor device".[4] As such, what is disclosed in Lee and Sakai apply to very distinct and mutually exclusive circuits of semiconductor devices. Even if both were incorporated on the same memory device, as the OFFICE ACTION alludes to[5], what is disclosed in Lee and Sakai would constitute very separate and distinct circuits, (i.e., Sakai would apply to a memory core and Lee would apply to circuitry that connects to the "I/O pad" and protects the memory device from electrostatic discharge) each having very separate and distinct design considerations. Thus, there simply is no logical reason or motivation of how one could possibly combine what is disclosed in Lee and Sakai and arrive at the transistor layout described in claim 23. To do so based on Applicant's own disclosure would be impermissible hindsight.

Thus, for at least these reasons, Applicants submit that claim 23 is not rendered obvious by Lee and Sakai.

[4] See Lee, column 1, lines 22-37.
[5] Page 10, lines 8-11, "it would have been obvious... to make both conductivity types to be present in the source/drain region of the Lee reference, as Sakai teaches, in order to be able to use Lee's structure in a memory device"